Теория сигналов и систем

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Power Efficient, Low Noise 2-5 GHz Phase Locked Loop

Предложено решение для системы фазовой автоподстройки частоты (ФАПЧ) с низким энергопотреблением и шумовыми характеристиками. Сигналы активации и деактивации ФАПЧ рассмотрены на системном уровне. Внедренная техника в значительной степени улучшает энергосбережение и уменьшает случайные изменения фазы. В результате удалось уменьшить затраты энергии и фазовый шум примерно на 35-38% при увеличении площади рабочей поверхности приблизительно на 17%.

A power and noise efficient solution for phase locked loop (PLL) is presented. A lock detector is implemented to deactivate the PLL components, except the voltage controlled oscillator (VCO), in the locked state. Signals deactivating/activating the PLL are discussed on system level. The introduced technique significantly saves power and decreases PLL output jitter. As a result whole PLL power consumption and output noise decreased about 35-38% in expense of approximately 17% area overhead.

Ключевые слова: *система фазовой автоподстройки частоты, понижение энергопотребления, дрожание частоты, статический ток, динамический ток.*

1. Introduction

Phase-locked loops are widely used in modern SoC and communication applications for clock and data recovery, frequency synthesis, frequency modulation, on-chip clock skew compensation, etc… [1-3]. Modern trends in constantly increasing data transfer rates impose rigorous requirements on noise and power parameters of PLL. Namely, clock jitter and signal phase distortions can seriously degrade the performance of analog and RF systems, causing information loss and glitches in digital systems [4]. Increase of data rates makes meeting jitter, phase noise and power consumption specifications more difficult. On the other hand, as transistor sizes scale down static power consumption drastically increases, as a result of this in modern technologies it becomes comparable to dynamic power consumption. This emphasizes the crucial need to decrease the power consumption of such fundamental block as PLL. In [5] the PLL power consumption was decreased by applying body biasing mechanism on transistors. However it is shown that in smaller technologies the biasing method losses its effectiveness [6]. In this paper a conceptually new application of power gating technique was suggested for PLL power consumption and noise reduction. The thorough analyses were performed for each of PLL blocks to decide the best gating type. Based on the performed analyses each PLL block was modified to support power gating.

2. Basic PLL architecture

The PLL used in this work is composed of five blocks (fig.1.): a phase-frequency detector (PFD), a charge pump (CP), a loop filter (LP), a voltage controlled oscillator (VCO) and a frequency divider (FD). PFD and CP are built based on classical topologies [4] widely used in frequency synthesizers. The loop filter is a second order passive filter built on CMOS varactors and polysilicon resistors. Its output *Vcnt* is the control voltage of the VCO. The VCO is based on four stage differential ring oscillator topology. The frequency divider is a 3 bit D-FF counter.

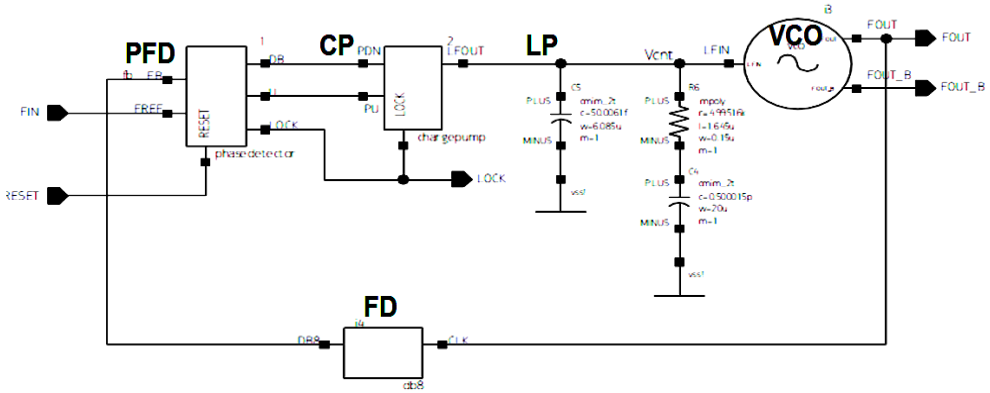


Fig. 1. PLL structure

Working frequency range of the PLL is 2-5GHz, with central frequency 3,5GHz. Design is realized in 45nm CMOS technology node with nominal supply voltage of 0,9V.

3. The suggested PLL power gating technique

As it is known PLL has two states: the acquisition state, when PLL changes its output clock frequency to be equal to reference clock and locked state when the output clock is aligned with reference signal, in frequency and phase. The working state of PLL is considered when it is locked. In this case the divider, PFD and CP are in “passive” state, when their inputs are mainly constant with minor deviations. The fig. 2 shows the activity of these blocks in locked and not locked states.

The activity of a block is defined as follows: its input voltage changes are observed for some time interval and the sum of the voltage changes is divided by the observation time. The activity equation can be written as:

$$A = \frac{\Delta V_{in1} + \Delta V_{in2} + \cdots + \Delta V_{inN}}{\Delta t}, \qquad (1)$$

where the ΔV_{inN} is the N-th block input voltage change of during the Δt observation time. Technically the block activity parameter denotes the amount of functionality performed by the block. As it can be seen from PLL component activity plots, their activity is close to zero when PLL is locked. Therefore in this condition these blocks only waste power and increase the whole system noise.

A new approach is proposed where all PLL blocks, except the VCO and CP, are being gated in lock condition. The issues rising here are detecting the locked state, gating the PLL blocks and reactivating of these blocks from the power down mode. The lock state of a PLL can be detected by means of the lock detector circuit. The lock detector reads the divider generated signal after 64 clock periods. If the divider generated frequency has not changed during the 64 periods, the PLL is assumed to be locked, and the circuit produces a positive lock signal. Having the lock signal a power gating mechanism can be developed. However another signal is needed to re-activate the system from power-down state. Such need can arise due to two reasons: the first and the main reason is that the PLL working conditions may experience changes, such as variations in reference clock, supply voltage or temperature fluctuations. The second is the tangible drop in the VCO control voltage, which may happen because of negligible leakage current in loop filter capacitors. This problem is actual for leaky CMOS technologies in fast processes (FF), high temperatures (>55C) and when PLL stays gated for a long time. This can be mitigated by using thick oxide (high voltage) MOS varactors as loop filter capacitors. To tackle these problems two control signals are required to be generated by PLL controlling system. The first is “system wake-up” which keeps track about the reference clock, PVT changes in the system, and if necessary re-actives the PLL from gated state. The second signal is “clock resynch”. It is activated when the gated system output clock needs to be refreshed. There are many ways to sense the VCO control voltage change to refresh the system. For example razor flops can be used as voltage change sensors [7]. The system can also be refreshed periodically, with time interval specific to it. Usually the time interval between system activations is very big and the clock refreshing time is negligible, which brings to insignificant power consumption during activation.

Fig.3 shows the architectural diagram of the proposed gating scheme.

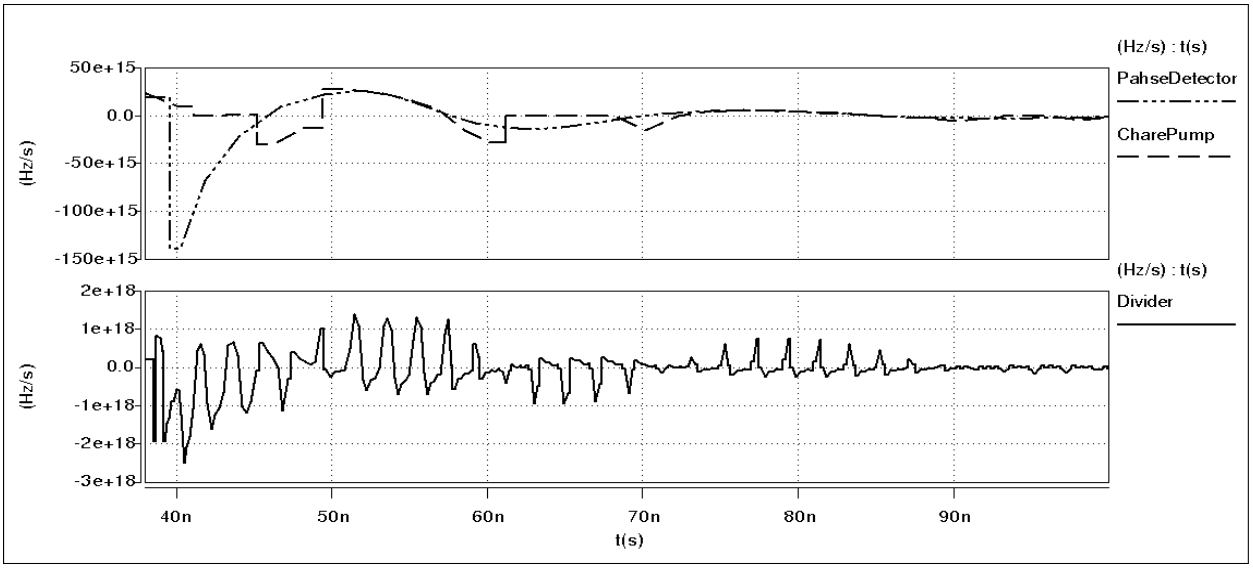


Fig. 2. PLL blocks activity vs. time

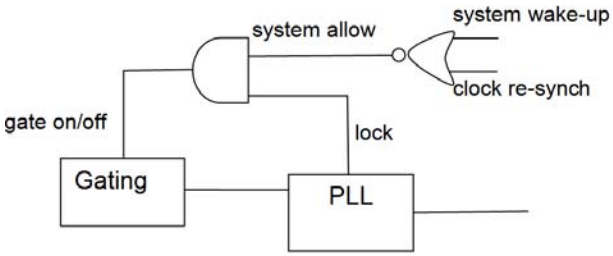


Fig. 3. Proposed PLL modifications

The default value of "system wake-up" signal is low, indicating that the system parameters have not changed; the default value of "clock re-synch" signal is also low, showing that the PLL output clock does not need in resynchronization. This causes the "system allow" signal to go high allowing the "lock" signal to gate the PLL blocks when the system is locked. The activation of any of the above mentioned signals reactivates the gated PLL blocks. The sleep transistors need to be chosen in a way to assure maximal power saving and minimal impact on the PLL. The second issue is connected with the choosing of the gating method. Using footer gating, header gating or both of them are the main options. The tradeoff between these methods is wake-up time, power saving and impact on the operation of the block. Besides, the gating transistors should be adequately large in order to be able to supply required current to the PLL. Otherwise the circuit operation will be seriously impacted in "slow" processes. This results in overall circuit area increase due to placement of bulky gating transistors.

In the next chapter each PLL block gating method will be discussed separately.

3.1. Frequency divider power gating

The divider consists of tree flip-flops and an inverter in its output. First thing that needs to be clarified while implementing the power gating is whether leave the clock to toggle in gated state or modify the PLL architecture so that the clock in divider input is also gated. Fig. 4 shows the supply rail static current for different gating methods in two cases when clock is active and passive.

As it can be seen from the figure clock deactivation decreases the power consumption in all observed corners. Based on this result the divider was modified to support clock deactivation in power gating mode.

Fig. 5. shows the divider current consumption for different power gating methods applied to the divider.

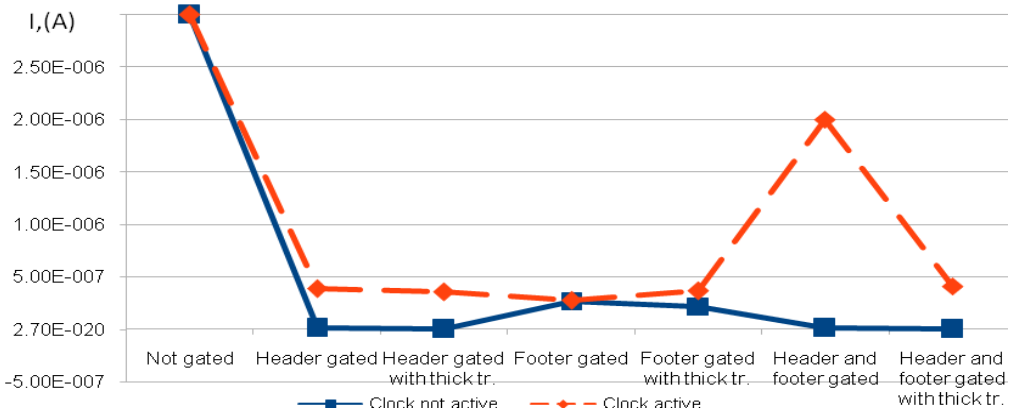


Fig. 4. Power saving due to clock gating

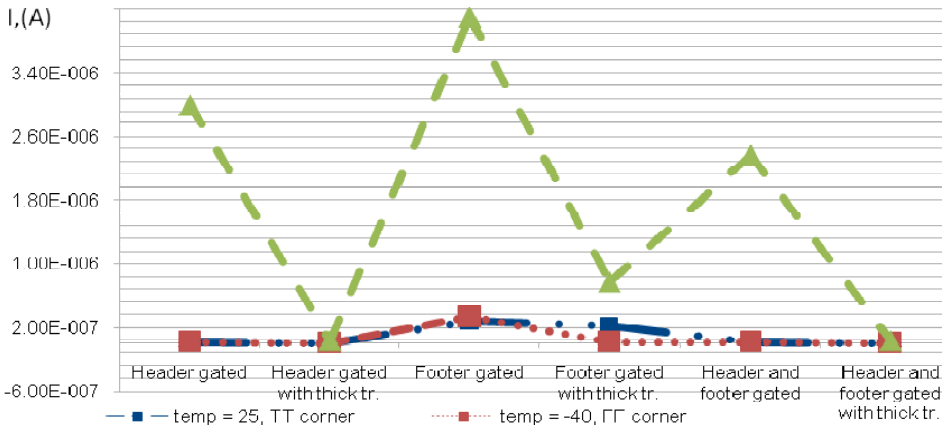


Fig. 5. Divider power gating simulation results

The vertical axis of the plot is the supply current, the horizontal axis is the gating. As it can be seen from the plot the best gating method for the divider is header power gating with thick oxide transistor.

3.2. PFD power gating

Fig. 6. shows the architecture of the phase detector. Lock detector, mentioned in paragraph 3 has been built into the PFD.

The simulation results of PFD current consumption values for different gating types are presented in fig. 7.

As it can be seen for PFD the best way of gating is header gating with tick oxide transistor.

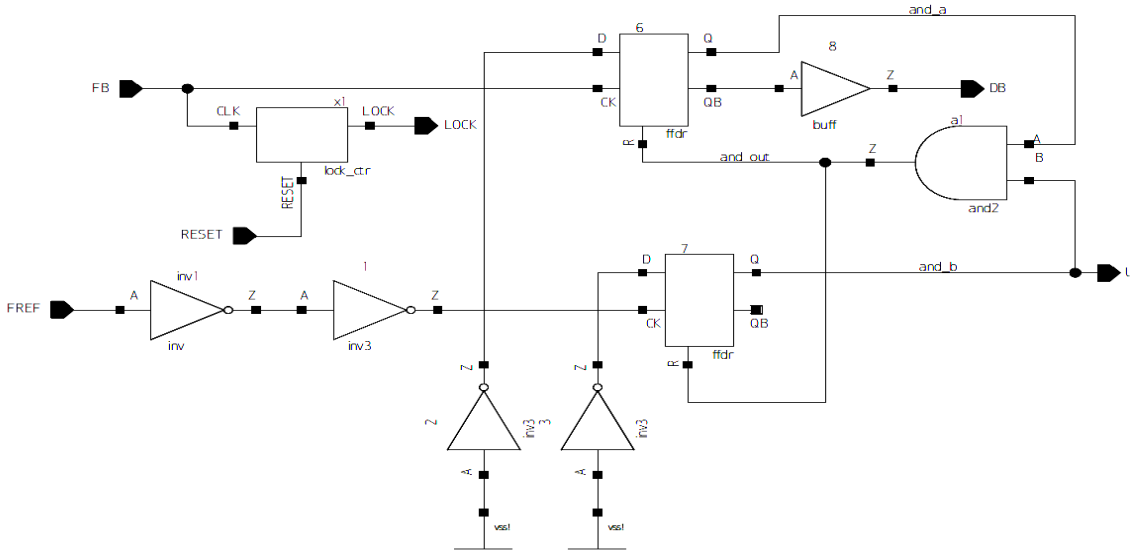


Fig. 6. PFD schematic

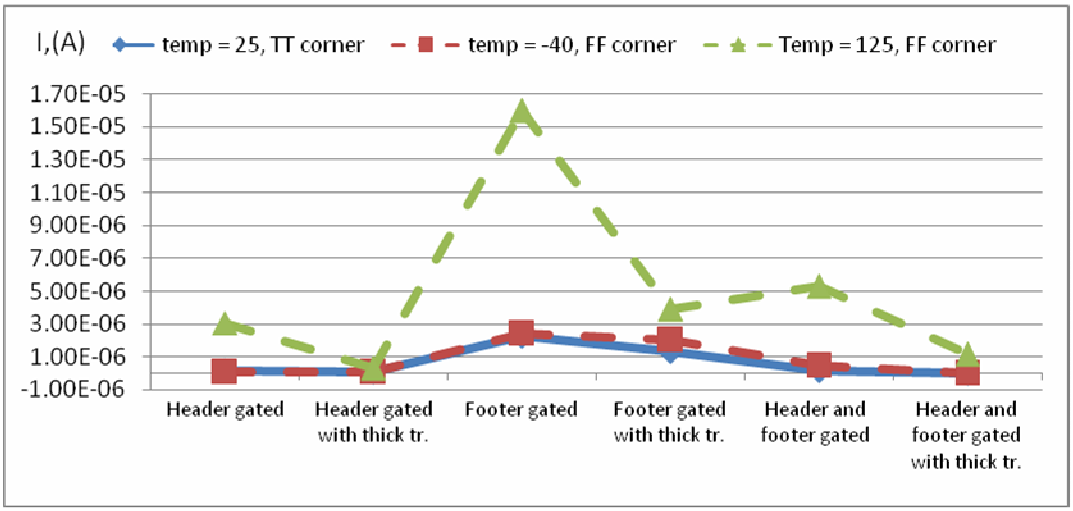


Fig. 7. PFD power gating simulation results

4. Jitter and Phase noise improvement

In essence the proposed PLL power-gating mechanism isolates the VCO and CP from the rest part of the circuit. This allows the oscillator operate free of influence of noise generated by switching processes in disconnected blocks. Digital components of PLL (PFD, frequency divider, etc...) are major sources of such harmful influences like simultaneously switching noise (SSN) [4]. This switching activity negatively affects the VCO output frequency stability and can dramatically increase the jitter.

Spikes of voltage on LF capacitors modulate VCO output frequency, increasing jitter. Isolating PFD keeps LF capacitors free of voltage spikes and hence eliminates additional frequency modulation of the VCO output. For a classical VCO:

$$f_{VCO} = kV_c\delta, \qquad (2)$$

where, k is the frequency gain of VCO. f_{vco} is the output voltage frequency of VCO. Where, if we replace the *Vc* control voltage (LF output) by $V_{cdc}+v_o(t)$, V_{cdc} is the noiseless DC component of the control voltage and $v_o(t)$ is the time dependent component representing noise of the loop filter

voltage, the resulting frequency (f_σ) can be rewritten as follows:

$$f_\sigma(t) = kv_\sigma, \quad (3)$$

$$f_{VCO}(t) = f_0 + f_\sigma(t), \quad (4)$$

f_o is noiseless frequency component. This simple expression shows that periodical voltage spikes of LF voltage causes PLL frequency to vary in time, i.e. introduces jitter.

5. Experimental results

The advantages of the proposed method are approved by the simulation results. The simulations were performed with HSPICE analog circuit simulator [8]. Figures 8(*a, b*) correspond to cases with and without PLL gating.

These figures represent output signal frequency spectrum. In fig. 8, *a* the carrier frequency (in solid circle) and two main frequency sidebands (VCO intrinsic phase noise, dashed circles) at -70db can be seen. While the fig. 8, *b* shows additional spurious frequency sidebands from frequency modulation by VCO input voltage fluctuations. The two main sidebands are also increased in value, reaching -58db. The difference between the two plots shows that the spurious frequencies are being effectively filtered out by isolation of LF-VCO Island. These results are also confirmed by cycle-to-cycle (CC) jitter measurement values. CC jitter is measured with help of the eye-diagram method. Eye plots for cases with and without power gating are considered, fig. 9 (*a,b*) correspondingly.

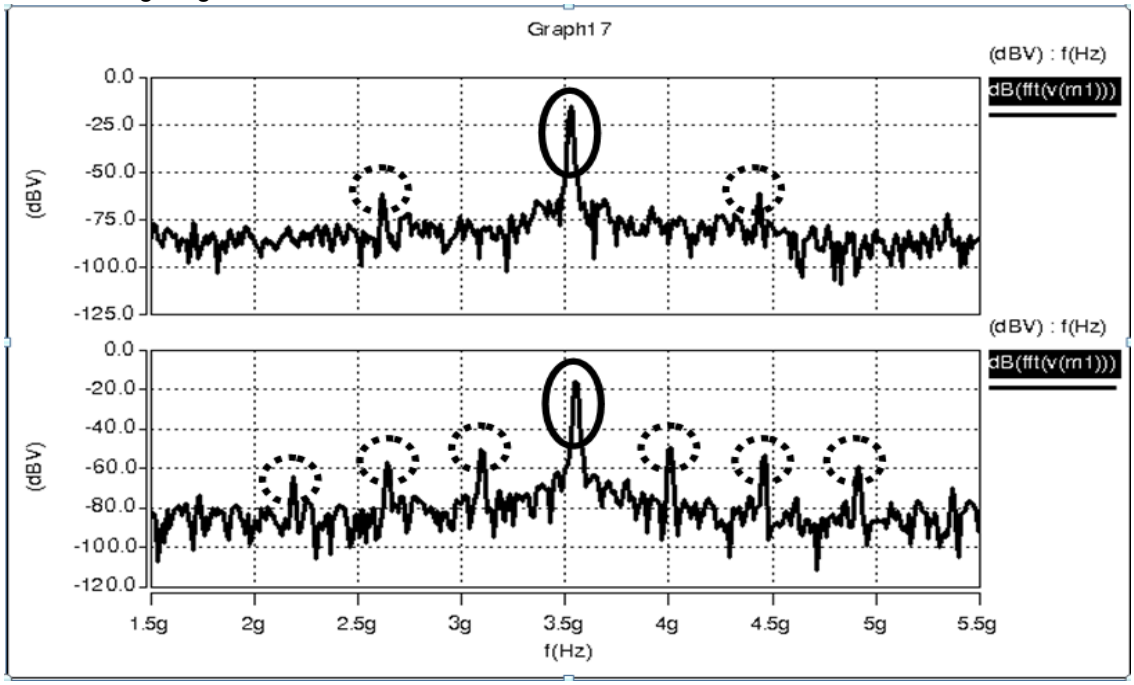
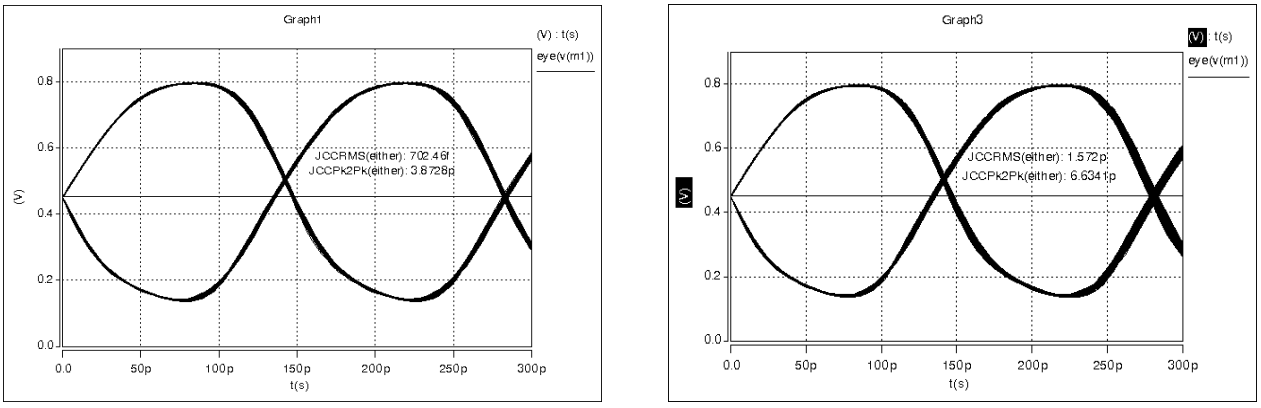


Fig. 8. *a*) VCO output frequency spectrum for gated PLL, *b*) VCO output frequency for not gated PLL



a ***b***

Fig.9. *a*) VCO output signal eye plots for gated PLL, *b*) VCO output frequency for not gated PLL

Results for CC jitter root main square (RMS) and peak-to-peak (pk2pk) values for PLL output signal at central frequencies are presented in the table.

Overall the whole power saving is more than 60%. However taking into consideration the dynamic power which is wasted on short periods of PLL re-activation, the whole power saving of the proposed method comes close to 37%. The results also show over 35% improvement of the PLL jitter.

Table 1.

		Divider			PFD		
		TT25	FF-40	FF125	TT25	FF-40	FF125
Power (W)	Not gated	2.4m	2.3m	7.8m	7.8m	3.6m	5.2m
	gated	3n	0.3n	20n	60n	30n	0.3u
	Avg power saving	80%			85%		
Noise		CC jitter pk2pk			CC jitter RMS		
	Not Gated	6.6ps			1.57ps		
	Gated	3.8ps			0.7ps		

Conclusion

In this work a power gating technique was applied on PLL for power and noise reduction. All PLL blocks, were discussed and the optimal gating type was chosen. After this the circuits were modified to support the chosen gating type. Detailed characterization for PLL in all critical corners was done, with the industry most precise analog simulator HSPICE.

As a result the suggested power gating method shows decrease of the overall PLL power consumption by about 35-38%, meantime it is decreasing the synthesized signal jitter by over 36.8%, in expense of up to 17% area overhead.

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