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Analysis of V_{TH} hopping power consumption method

В статье предложена энергетическая модель для V_{TH} прыжковой схемы, получены уравнения для расчета уменьшения энергии. На основе продложенной модели формально сформулирована задача V_{TH} прыжковой схемы, для решения которой использован эвристический алгоритм. Показано, что при использовании этого метода можно сохранить примерно 30% статической энергии при увеличении площади схемы не более чем на 3%.

An energy saving model for V_{TH} hopping scheme was proposed. The appropriate energy saving equations were calculated. Based on that model the V_{TH} hopping problem was defined and heuristic algorithm was used for that problem resolving. Nearly 30% static power saving was achieved using this method, while the area overhead is less than 3%.

Introduction

As circuit design moves to smaller technology nodes the standby power dissipation of devices is becoming a critical concern. Even more in recent technologies 32nm or below the static power consumption is more than dynamic power consumption. In fact in modern chips the leakage power can be responsible for 40% or more of the total system power [1, 2]. Therefore circuit leakage control is crucial for both high performance and low power design systems.

All currently existing power reduction techniques can be classified in two main groups: dynamic power reduction techniques and static power reduction techniques. These two methods have some similarities; they both look for circuit idleness; however it is very complicated to apply these two methods on the same time, because all dynamic power reduction methods are one cycle based methods. In contrary to this the static power reduction methods require more than one clock cycle circuit idleness, to be sure that power consumed on circuit gating is smaller than the saved power during gating period.

In this work analytical equation for one of static power reduction techniques, VTH hopping, was presented. A formal VTH hopping problem was formulated and heuristic method was used to solve that problem. The initial target of problem formulation was to apply VTh hopping on clock cycle bases.

General overview of V_{TH} hopping

V_{th} hopping is one of the most aggressive technologies for dramatically reducing the leakage power in circuits. The general V_{th} hopping scheme is brought on figure 1.

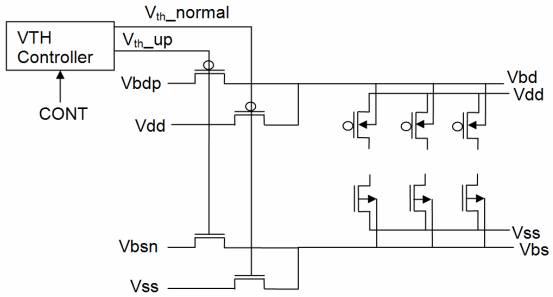

Fig. 1. V_{TH} hopping scheme

The CONT signal being formed from processor software or internal circuitry generates either Vth_up or Vth_normal signals. When Vth_up is logic high then the threshold voltage of transistors is increasing, which brings to decrease of circuit leakage current, and when Vth_normal is assigned then the threshold voltage of transistors returns to their normal values allowing transistor nominal performance.

For being able to correctly calculate static power saving during the V_{TH} hopping, an accurate energy saving model as function of time is required ($E_S(t)$). Traditionally the $E_S(t)$ estimation was performed assuming that circuit leakage is being decreased by constant K factor when the circuit enters to low leakage state. Hence the total energy saving would be

$$E_S(t) = E_{leak}^{normal}(1-K) \qquad (1)$$

where E_{leak}^{normal} is the circuit energy in the normal state.

However such assumption is not correct as the leakage reduction is not a immediate effect and the circuit needs some time for decreasing it's leakage current to minimal value after entering to its low power state. For example in fig. 2(a) is shown a diagram of applying V_{TH} hopping to feedback trigger.

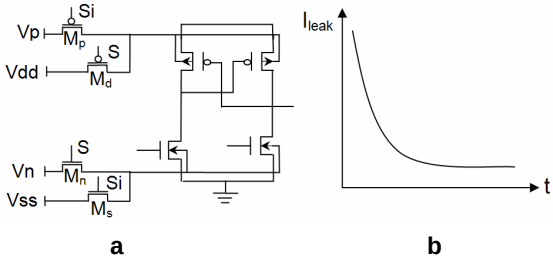

Fig.2. Leakage reduction process in V_{TH} hopping

When select (S) signal is assigned the M_s and M_d transistors are gradually switching off, meantime M_p and M_n transistors are turning on. This process brings to increase of feedback transistors body voltages, which brings to decrease their

threshold voltages. Therefore the overall sub-threshold current is decreasing. In fig 2(b) the leakage current behavioral diagram is brought. As can be seen from that diagram the leakage current is not decreasing immediately at the initial stage of Vth hopping it decreases rapidly and after some time it reaches to its final value. This shows that the leakage or the same is energy reduction K factor is decreasing gradually after entering into low power mode, and after some time it reaches to its maximal value. Hence the energy estimation with (1) equation introduces spurious results during the V_{th} hopping and it is a optimistic energy saving model.

For leakage reduction techniques used in standby mode, this error is negligible since the circuit downtime is pretty long. However for V_{th} hopping the circuit downtime is usually short and state transition happen frequently. In this case this error is not negligible. Accurate estimations of energy saving are essential to make design trade-offs for V_{th} hopping.

In recent researches it is paid more attention for modeling of V_{th} hopping. In [4] a new adaptive body biasing method was proposed, which mainly relies on empirical calculations of energy savings during body biasing. In [5] a body biasing method and dynamic voltage scaling methods were incorporated with each other, and in this work energy saving models for both methods were proposed which mainly relies on probability distribution function.

Summarizing the estimation of energy saving during V_{th} hopping is very important for correct design trade-offs.

Energy saving equation for V_{TH} hopping

In this section we derive an accurate energy calculation equation for V_{th} hopping scheme. From fig 2(a) when V_{th} hopping is applied M_s and M_d transistors are switching off, while Mp and Mn transistors are switching on. The energy overhead (E_{ov}) for switching these transistors on/off is

$$E_{OV} = 4 * C_F * V_{DD}^2 \qquad (2)$$

Where C_F is the gate capacitance of hopping transistors and V_{DD} is supply voltage. Assuming the original leakage current in circuit without applying V_{th} hopping is equal to I_{orig} and the current after hopping is equal to I_{hop} the overall energy saving during the t time after applying V_{th} hopping will be

$$E_{hopping}(t) = -4C_F V_{DD}^2 + V_{DD}(I_{orig} - I_{hop})t \qquad (3)$$

To quantify the leakage current after applying threshold hopping the three major effects needs to be studied.

1) Charging of internal nodes.

When the circuit transistors are body biased their threshold voltages are increasing which brings to decrease of leakage current. As transistor leakage current is decreasing and transistor resistance is increasing this will bring to increase of circuit internal node potentials. The increase of the node potentials will bring to charging of circuit nets parasitic capacitances. Assuming that the total node capacitance is C_{int} this charging process can be characterized by

$$V_{int}(t) = \frac{1}{C_{int}} \int_0^t I(t)dt \qquad (4)$$

2) Sub-threshold leakage reduction

As the potential of internal nodes are increasing after V_{th} hopping is applied, this brings to decrease the voltage difference between the transistor contacts; overall the transistor leakage is reducing also. In [3] the sub-threshold leakage of transistor is given by

$$I = A * e^{1/mv_T (V_G - V_S - V_{th0} - \gamma' V_S + \eta V_{DS})} * (1 - e^{-V_{DS}/V_T})$$
$$A = \mu_0 C_{ox}' \frac{W}{L_{eff}} (V_T)^2 c^{1.8} c^{-\Delta V_{th}/\eta v_T} \qquad (5)$$

Where V_{th0} is the zero bias threshold voltage, V_T is the thermal voltage, γ is the linearized body effect coefficient and η is the DIBL coefficient.

The foregoing equation can be used to calculate the leakage reduction of each transistor. In [8] work is proven that total leakage (I_{leak}) of gate can be approximated into an exponential function of it's virtual ground (V_{VG})

$$I_{leak} = I_0 e^{-K_{gate} V_{VG}} \qquad (6)$$

Where K_{gate} is the leakage reduction exponent of the gate and I_0 is zero V_{VG} leakage current.

3) Circuit self-charging

When V_{Th} hopping is applied to a single transistor the potential of bulk is starting to increase, this brings to charging of drain-bulk and source-bulk parasitic capacitances, which brings to increase in leakage current. Assuming that the resistance of hopping transistor is equal to R, the potential of hopping b point can be calculated with below equation

$$\Delta V_b(t) = (V_P - V_{DD})(1 - e^{\frac{-t}{RC_b}}) \qquad (7)$$

Where $\Delta V_b(t)$ is the increment of the P substrate voltage and C_b is the total capacitance of P substrate.

Based on all stated effects the body-biasing scheme for single transistor can be modeled as fig. 3

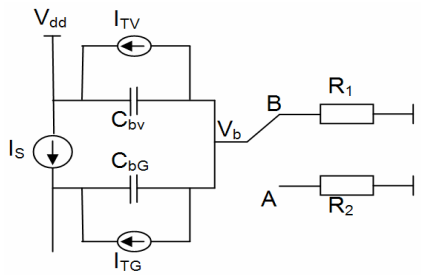

Fig. 3. Model of transistor V_{TH} hopping scheme

Where I_S is the sub-threshold leakage, I_{TG} is substrate to ground BTBT leakage and I_{TV} substrate to V_{DD} leakage. C_{bv} and C_{bg} are respectively substrate to ground and substrate to V_{DD} capacitances. Based on this scheme and using KCL low we calculate the overall energy saving equation for V_{th} hopping scheme

$$E_S(t) = V_{DD}(I_S + I_T)t - C_C V_p^2 - E_{bias}(t) - E_{Vdd}(t) \quad (8)$$

Where I_S and I_T are total sub-threshold and BTBT leakage current of circuits without threshold hopping, C_C is the gate capacitance of control transistors, $E_{bias}(t)$ is the energy consumption of bias voltage source, E_{Vdd} is energy consumption of V_{DD}.

Modeling V_{TH} hopping

In this section calculate the energy breakeven time (EBT) and wake-up times (WUT) for V_{TH} hopping scheme will be calculated. When V_{TH} hopping is applied the V_b switches from V_{DD} voltage to V_P voltage, the energy consumed during this switching process is equal to

$$E_{Swt} = V_p^2(C_1 + C_2) \quad (9)$$

For fully charging the PMOS transistor body is equal to

$$E_{charging} = (C_{bG} + C_{bV})\Delta V_p^2 + C_{bG} V_{DD} \Delta V_P \quad (10)$$

The total leakage reduction after the body charging will be

$$I = e^{B_S \Delta V_p} I_s + e^{-B_{ts} \Delta V_p} I_t \quad (11)$$

Where I_s and I_t are original sub-threshold leakage and BTBT leakage of the circuit without V_{TH} hopping. The energy saving per unit time is

$$E_{saving/ut} = (I_s + I_t - I) * V_{DD} \quad (13)$$

Based on these equation the EBT and WUT time can be calculated by

$$T_{EBT} = \frac{E_{swt} + E_{charging}}{E_{saving/ut}} \quad (14)$$

$$T_{WUT} = \frac{(C_{bg} + C_{bv})\Delta V_p}{I_2} \quad (15)$$

Algorithm for V_{TH} hopping

The following parameter needs to be determined for successfully V_{TH} hoping biasing voltages, hopping transistor sizes and hopping gate selection. If the sum of EBT and WUT times, defined as EAW, can be reduced one clock cycle then V_{TH} hopping mechanism can be applied on clock cycle bases.

Based on all up stated equation the final V_{TH} hopping problem can be defined as following

Calculate: S_1, S_2, S_3, S_4, Vp, V_n

Maximize: $E_{saving/ut}$ (16)

Constraint: $T_{EAW} \le T_{clk}$

Experimental results

The V_{Th} hopping problem (15) was modeled with computer program and heuristic method was used for resolving it.

V_{TH} hopping was applied on an inverter chain with 32nm and 45nm technology for 32nm technology the leakage reduction was nearly 32% and the area overhead 1.7%. For 45nm technology the leakage reduction was 38% and area overhead was 5.5%.

Table 1 shows the V_{TH} hopping method applied to different type of circuits.

Table 1

Circuit	Area overhead %	Leakage red. %
D-flipflop	1.2%	26%
Decoder	0.6%	30%
ALU	0.6%	27%
Multiplier	1%	35%
ECAT	1.4%	51%

Based on performed experiments dramatically reduction of the average static leakage was observed in cost of very small area overhead.

Conclusion

In this paper an analytical equations for calculating the V_{TH} hopping energy saving, energy breakeven and wake-up time was presented. A formal V_{TH} hopping problem was formulated. Based on the received equation and problem formulation the heuristic programming method was proposed for resolving the problem.

Based on performed experiments, dramatically reduction of the average static leakage power was observed in cost of negligible area overhead.

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