Силовая электроника

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Alexey Tyshko, NATA Consulting LLC,
729 Meadowbrook Drive, Coatesville, PA 19320, USA.

Excitation of the resonant loads with the multi-vector synthesized sinusoidal voltage decreases conduction losses and improves reliability

A method of DC/AC conversion based on the multi-vector synthesis of the sinusoidal voltage with the sequential elimination of unwanted harmonics in the output voltage and current resulting in lower power dissipation especially for the resonant loads is discussed. Simulation results of the standard 50% duty cycle operation approach and the proposed multi-vector topology are compared and linked to the temperature related characteristics of the MOSFET switches and resulting life expectancy of the DC/AC inverter. Ref.12, Figs. 6, tab. 1.

Keywords: *conductive losses, DC/AC converter, high harmonics, MOSFET high temperature characteristics, multi-vector method, resonant loads, sine voltage synthesis.*

Introduction

Continuous efforts to increase efficiency of the power generating and converting systems and modules are pushed not only by the growing cost of the energy but also by other considerations such as the reliability depending on the components operating temperature. According to the Arrhenius law which is applicable to the electronic components [3] every 10°C increase of the operation temperature decreases component life expectancy in half.

Power components losses generate heat which becomes a significant problem especially in the space constrained high temperature operating equipment [8]. For the industrial frequency operation any type of the existing power switches such as thyristors, GTO, IGBT or bipolar transistors may be used, but for the frequencies over 100kHz MOSFETs are the preferable ones.

MOSFET switch losses include two main components – switching and conduction. While the switching losses may be significantly reduced by using ZVS/ZCS modes of operation the conduction losses may be the biggest source of heat to be dealt with. MOSFET conduction losses are proportional to the channel resistivity R_{dson} and RMS current. Early paper on the dependency of R_{dson} on die temperature found an additional dependency upon the drain current [5]. Results of the more extensive research covering temperature range up to 200C and drain current effect (Fig. 1) are provided in [9] and [10].

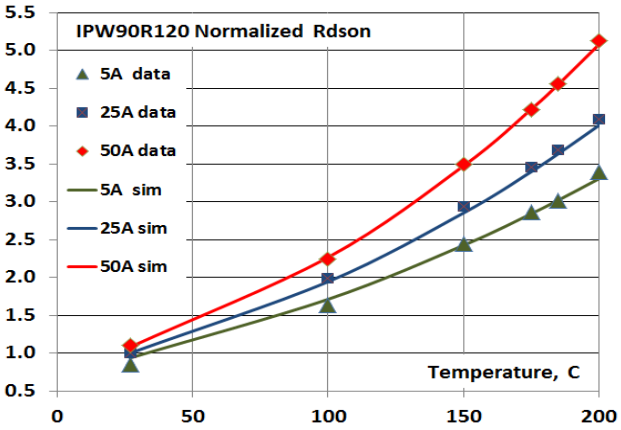

Fig. 1. Normalized R_{dson} vs. temperature and drain current [10]

The normalized changes of R_{dson} shown on Fig. 1 vs. two parameters - the die temperature T and the drain current I may be described as following

$$R_{DS(on)}(T,I) = R_{DS(on,test)} \times \left[1 + a\left(\frac{I}{I_{test}} - 1\right)\right] \times \left(\frac{T}{300}\right)^{b+\frac{cI}{I_{test}}} \quad (1)$$

where I_{test} is a test current from the datasheet, while parameters a, b and c are found following the standard fitting procedure to maximize the correlation factor based on the manufacturer datasheet [2] and some experimental points [10].

The same drain current produces 3 to 5 times more power at 200C compare to 25C and with poor thermal management it can trigger a thermal runaway ending in the catastrophic failure or at least it decreases total inverter reliability and its expected life time [3].

For the special high temperature equipment operating in the ambient temperature range 150C to 175C with very narrow margin for the temperature rise providing a heat flow from the power component to the ambient every watt of dissipated power is critical. Any sound attempt is welcomed to

decrease the power dissipation per each MOSFET. Use of multiple switches connected in parallel to share both current and dissipated power is a common practice.

This paper describes an approach based on the multi-vector sine wave synthesis providing selective cancelling of the higher harmonics in the output voltage of DC/AC convertor and significantly reducing related to the higher harmonics power dissipation while operating with the resonant loads.

1. Switch mode inverter operation with the resonant load

High efficiency DC/AC converters operating with the resonant loads include the switch mode stages (PWM Inverter) and a series filter between the output of the inverter and a resonant load as shown on Fig. 4. The inverter output voltage usually has a negligible switching time compared to the period of the output operating frequency. To produce maximum power a square wave 50% duty cycle voltage is generated containing only odd harmonics with the amplitudes Vn defined by Fourier equation [6] where n is a harmonic number and φ is a half-width of the rectangular pulse with the amplitude V_0

$$V_n = V_0 \frac{4}{\pi n} \sin(n\varphi) \qquad (2)$$

Useful is only the fundamental harmonic producing output voltage at the resonant load while the rest of harmonics generate currents which are simply shorted to the ground. High harmonic currents in some cases may exceed the fundamental one and they may produce a significant heat in the power components. A series output filter Lf, Cf tuned to the fundamental frequency limits high harmonic currents. Filter optimization is always a delicate balance between the filter bandwidth allowing fast changing (modulation) of the output voltage (Lf minimized) and high harmonics currents limiting (Lf maximized).

2. Harmonic cancellation using phase shifted vectors

Classic problem with the third harmonic cancellation for the electrical motors has a simple solution - two 60° shifted voltages cancel third harmonic [6]. Other methods include multiple switch mode inverters combining their output voltages with different amplitudes or frequencies [1], [4], [6]. Discussed multi-vector approach allows cancelling of multiple unwanted harmonics by combining the same amplitude and frequency 50% duty cycle phase shifted voltages forming a quazi-sinusoidal voltage [11] as shown of Fig. 2.

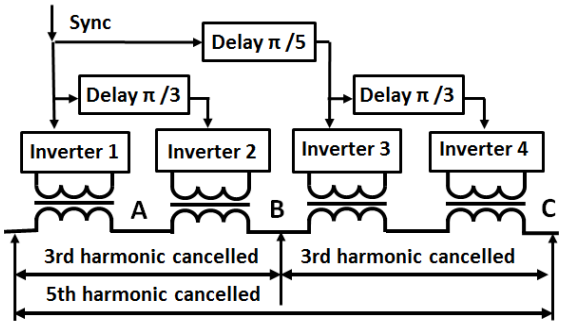

Fig. 2. Inverter topology cancelling 3rd (B) and 5th (C) harmonics [11]

Resulting combined output voltages to form a sinusoidal signal at the load are shown on Fig. 3. Marker A refers to the original 50% duty cycle voltage at the output of each inverter, B refers to the voltage without 3rd harmonic and C refers to the voltage without 3rd and 5th harmonics. Sine voltage is restored at the load.

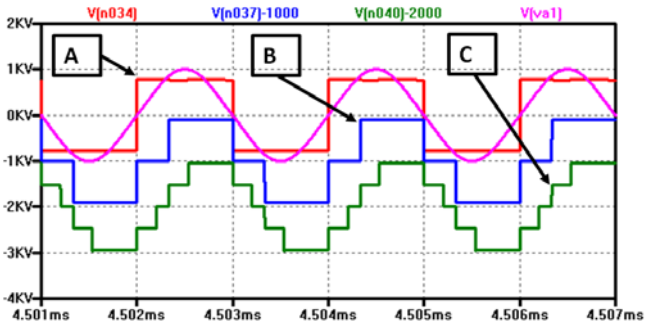

Fig. 3. Original 50% duty cycle inverter output signal A, modified inverter with cancelled 3rd harmonic B and inverter with cancelled 3rd and 5th harmonics C

3. Simulation Results and Discussion

Simulated schematic shown on Fig. 4 is configured to produce A, B or C output voltages (Fig. 3) depending on the control signals phase shifts between the half-bridge output stages following Fig. 2 diagram.

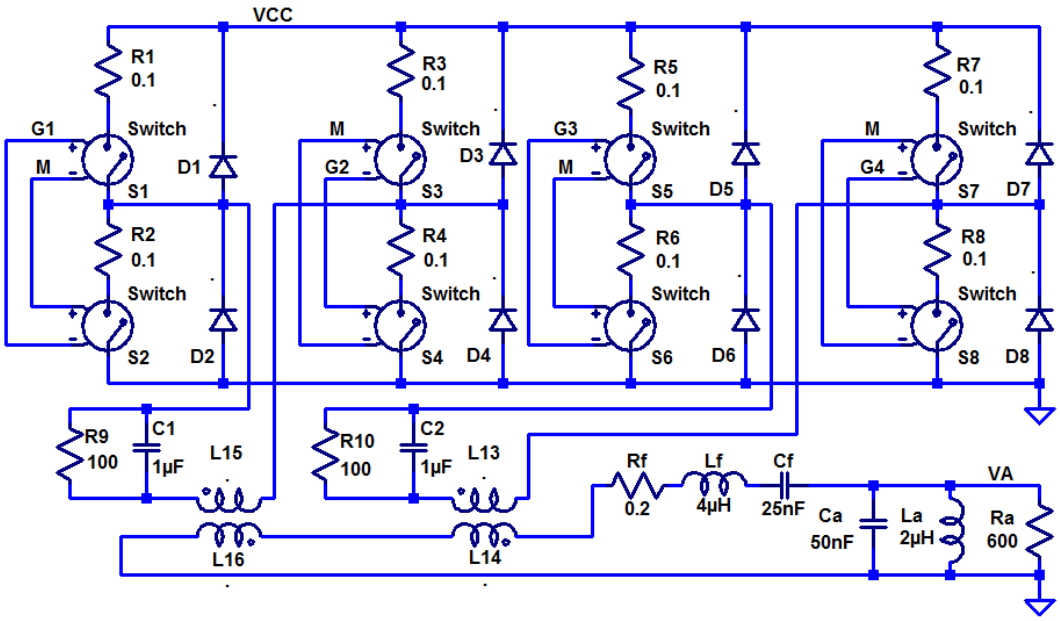

Fig. 4. Secondary windings (series filter) currents for A, B, C configurations

MOSFET switches conduction losses are calculated based on series resistors 0.1ohm representing Rdson of used IPW90R120 at 25C die temperature or 0.3ohm for 175C according to Fig. 1. MOSFET temperature rise due to the conduction losses is based on the known die to ambient thermal resistance 5C/W. Resulting life expectancy decrease is shown in Table 1.

Due to different content of the first harmonic the output transformers turns ratio is adjusted for each configuration to provide 1000Vp at the load while operating from 600V bus voltage [8], [11]. Resulting filter current is shown on Fig. 5.

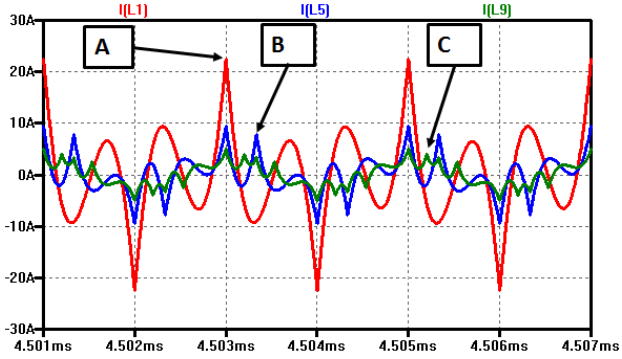

Fig. 5. Secondary windings (series filter) currents for A, B, C configurations

Tables 1.

Schematic configuration	A	B	C
Output voltage, Vpeak	1000	1000	1000
Output transformer ratio	2x0.642	2x0.751	2x0.791
Relative output transformer ratio	1	1.17	1.23
Filter current, A peak	22.7	9.6	5.06
Filter current, A rms	8.22	3.33	2.1
Switch current, A rms	5.31	2.61	1.79
Switch power dissipation for Rdson 0.1ohm @ 25C	1.41	0.34	0.16
Switch power dissipation for Rdson 0.3ohm @ 175C	4.22	1.02	0.48
Temperature rise for Rth 5C/W @ 175C	21.1	5.1	2.4
Life expectancy decrease compare to 175C, times	4.3	1.4	1.2

The output transformer ratio is corrected to compensate first harmonic change.

4. Amplitude control

Synthesized sine voltage is proportional to DC bus voltage feeding inverters. To regulate load voltage from zero to the maximum without affecting low harmonic content two synthesized identical voltages with symmetrical phase shift should be combined following the Chireix outphasing method [7], [11], [12] as shown on Fig. 6.

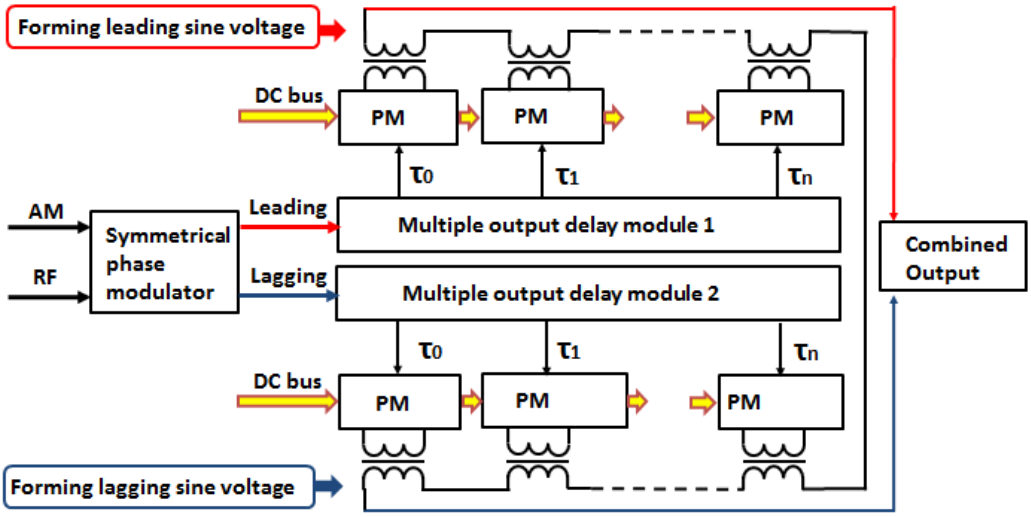

Fig. 6. Multi-vector outphasing topology with regulated output voltage [11]

Conclusions

In this paper a multivector method of sine voltage synthesis is analyzed for operation with the high Q resonant loads based on LTSpice simulation of different inverter topologies including the same 8 MOSFET switches. The sequential cancellation of the higher harmonics significantly reduces the power dissipation per MOSFET and increases reliability and life expectancy especially at high ambient temperature of 175C up to 4 times according to Arrhenius law.

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А. Тишко, NATA Consulting, LLC,
729 Meadowbrook Drive, Coatesville, PA 19320, USA.

Збудження резонансної нагрузки синусоідальною напругою синтезованою багатовекторним методом знижує втрати і підвищує надійність

Показано перевагу застосування багатовекторного методу сиртезу синусоідальної напруги з подавленням вишчих гармонік при роботі на резонансну нагрузку. Для перетворювачів працюючих при дуже високій температурі (175С) виграш в очікуваном часі життя може бути 3 – 4 рази за правилом Ареніуса при тій самій кількості силових транзисторів. Бібл. 12, рис. 6, табл. 1.

Ключові слова: *втрати провідності, перетворення напруги постійного струму в зміний, вищі гармоники, багатовекторний метод синтезу, резонансна нагрузка, синусоідальна напруга, високотемпературні характеристики польових транзисторів.*

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А. Тышко, NATA Consulting, LLC,
729 Meadowbrook Drive, Coatesville, PA 19320, USA.

Возбуждение резонансной нагрузки синусоидальным напряжением синтезированным многовекторным методом снижает потери проводимости и увеличивает надежность

Показано преимущество использование многовекторного метода синтеза синусоидального напряжения с подавлением высших гармоник при работе на резонансную нагрузку. Для преобразователей работающих при очень высоких температурах (175С) выигрыш в ожидаемом времени жизни может достигать 3 – 4 раза по правилу Аррениуса при том же количестве используемых силовых транзисторов. Библ. 12, рис. 6, табл. 1.

Ключевые слова: *потери проводимости, преобразование постоянного напряжения в переменное, высшие гармоники, многовекторный метод синтеза, резонансная нагрузка, синусоидальное напряжение, высокотемпературные характеристики полевых транзисторов.*

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